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Authors	NALDI, Giovanni, COMORETTO, Giovanni, Chiello, Riccardo, Pastore, Sandro, PUPILLO, Giuseppe, MATTANA, Andrea, MELIS, Andrea, CONCU, Raimondo, ALDERIGHI, MONICA, Aminaei, A., Baker, J., BELLI, Carolina, CHIARUCCI, Simone, D'ANGELO, SERGIO, Dalle Mura, G., De Marco, A., Halsall, R., Magro, A., MONARI, JADER, NAVARRINI, Alessandro, PERINI, FEDERICO, POLONI, MARCO, Roberts, M., RUSTICELLI, SIMONE, SCHIAFFINO, MARCO, SCHILLIRO', FRANCESCO, Zaccaro, E., Zarb Adami, K.
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Development of a new digital signal processing platform for the Square Kilometre Array

G. Naldi*⁽¹⁾, G. Comoretto⁽²⁾, R. Chiello⁽³⁾, S. Pastore⁽⁴⁾, G. Pupillo⁽¹⁾, A. Mattana⁽¹⁾, A. Melis⁽⁵⁾, R. Concu⁽⁵⁾, M. Alderighi⁽⁶⁾, A. Aminaei⁽³⁾, J. Baker⁽⁷⁾, C. Belli⁽²⁾, S. Chiarucci⁽²⁾, S. D'Angelo⁽⁶⁾, G. Dalle Mura⁽⁸⁾, A. De Marco⁽⁹⁾, R. Halsall⁽⁷⁾, A. Magro⁽⁹⁾, J. Monari⁽¹⁾, A. Navarrini⁽⁵⁾, F. Perini⁽¹⁾, M. Poloni⁽¹⁾, M. Roberts⁽⁷⁾, S. Rusticelli⁽¹⁾, M. Schiaffino⁽¹⁾, F. Schillirò⁽¹⁰⁾, E. Zaccaro⁽⁸⁾, K. Zarb Adami^{(3),(9)}

(1) INAF, Institute of Radio Astronomy, Bologna, Italy; e-mail: gnaldi@ira.inaf.it

(2) INAF, Astrophysical Observatory of Arcetri, Florence, Italy; e-mail: comore@arcetri.astro.it

(3) University of Oxford, Department of Physics, Oxford, United Kingdom; e-mail: riccardo.chiello@physics.ox.ac.uk

(4) Sanitas EG, Milan, Italy; e-mail: sandro.pastore@sanitaseg.it

(5) INAF, Astronomical Observatory of Cagliari, Selargius (CA), Italy

(6) INAF, Institute of Space Astrophysics and Cosmic Physics, Milan, Italy

(7) Science & Technology Facilities Council, Rutherford Appleton Laboratory, Harwell Campus, Didcot, United Kingdom

(8) Campera ES, Via Mario Giuntini 13, 56023, Navacchio, Pisa, Italy

(9) University of Malta, Institute of Space Sciences and Astronomy, Msida, Malta

(10) INAF, Astrophysical Observatory of Catania, Catania, Italy

Abstract

A novel digital hardware platform has been designed for the Low Frequency Aperture Array (LFAA) component of the Square Kilometre Array (SKA). This board, called Analog Digital Unit (ADU), is a 6U board containing sixteen dual-inputs Analog to Digital Converters (ADC) and two Field Programmable Gate Array (FPGA) devices, capable of digitizing and processing 32 RF input signals. We present the main features of the board and the signal processing firmware that has been developed for LFAA. Although the ADU has been conceived mainly for the low frequency band (50-350 MHz), its use has been proved effective also for higher frequencies (375-650 MHz). In this paper we describe also the application of ADU as the digital acquisition and processing system for PHAROS2, a cryogenically cooled 4-8 GHz Phased Array Feed (PAF) demonstrator. The final part is focused on the future developments of the board.

1. Introduction

The LFAA component of the SKA, in the first phase, will be composed of 2^{17} log-periodic antennas, grouped in tiles of 16 antennas each [1]. Each tile is processed in a Tile Processing Module (TPM), and 16 TPMs are connected in a flexible way to form a logical station, which is an aggregation of 256 antennas, using a general purpose high speed Ethernet interconnect.

The National Institute for Astrophysics (INAF) plays a fundamental role in the design of the LFAA system. In this context, an Italian version of the TPM (iTPM) has been proposed and, in particular, a new digital board (ADU) for the iTPM has been developed in collaboration with Sanitas EG, University of Oxford, Malta University and Science and Technology Facility Council (STFC).

The iTPM consists of two units. The first, called Pre-ADU board, performs analogue conditioning of the signals coming from 8 dual polarization antennas. The second unit is the ADU, that is capable of acquiring and processing the broadband (up to 500 MHz bandwidth) radio-frequency streams from 16 dual polarization antennas (32 analogue signals). Data processing includes channelization of the sampled data for each antenna, correction for instrumental response and for geometric delays and formation of one or more beams by combining the aligned streams. An iTPM is, thus, an assembly of one ADU and two Pre-ADU boards. A picture of the iTPM assembly is shown in Figure 1.

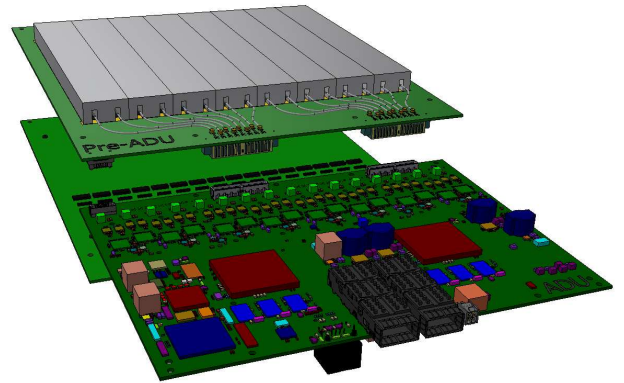


Figure 1. 3D CAD drawing of iTPM assembly showing two Pre-ADU(s) and one ADU.

It is envisaged that there will be 8192 of these signal processing platforms in the first phase of LFAA, so great efforts have been made to ensuring the design is low cost and low power.

The current release of iTPM assembly has been used as part of the Aperture Array Verification System (AAVS) demonstrator, that will be realized with the deployment of 400 antenna prototypes at the Murchison Radio-

astronomy Observatory (MRO, Western Australia). At the moment only 256 antennas have been installed on site.

2. Hardware Overview

The ADU board [2] (Fig. 2) is the hardware component that carries out digitization and signal processing functions. Even if it has been conceived to be assembled with Pre-ADU boards, it can be used with any analogue receiver system through a suitable 50 Ohm high-isolation RF connector (as described, for example, in Section 4.1).

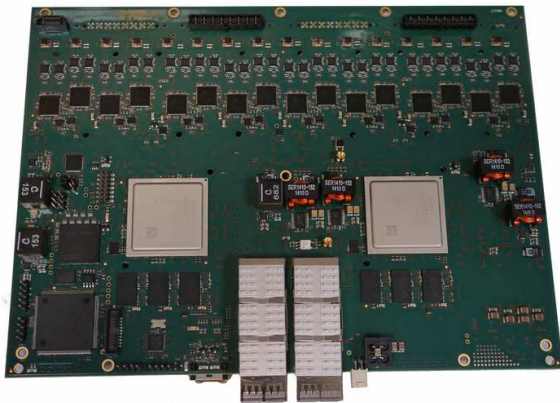


Figure 2. Top view of the ADU board.

The 32 RF analogue input signals are converted from single ended to differential signals by baluns and digitized by sixteen 14-bits dual-input ADCs, that send the eight most significant bits to the FPGAs via high speed serial interface supporting JESD204B data transmission protocol.

The selected device for AD conversion is the AD9680 of Analog Devices Inc. enabling a sampling rate up to 1GSPS of dual inputs. The FPGAs of the board are two Xilinx 20 nm Kintex UltraScale XCKU040 devices.

Other relevant characteristics and features of the board are the following:

- Compact size, 6U format compatible.
- Advanced 14-layers board build-up.
- Twelve DDR3 memory chips supporting 1.5 GByte of memory and 96-bit wide memory bus. The maximum bitrate is 1600 Mbps.
- FPGA to FPGA fast link for transferring data from one FPGA to the other. It consists of 36 LVDS lanes supporting up to 1.6 Gbit/s per lane.
- 40 GbE QSFP+ interface (one per each FPGA) using four high speed transceivers.
- Low-level Ethernet Gigabit management interface with instant ON Flash-based Lattice CPLD.
- Complete system monitor interface with power, voltage and temperature monitoring.
- SPI interface for programming ADCs, PLL and Pre-ADU boards.

- Highly efficient multistage power distribution system, with configurable start up sequence and selective function related power control capability.

The estimated power budget of the ADU board is about 155 Watt.

In Fig. 3 it is reported a schematic diagram showing the main functional blocks of the ADU board.

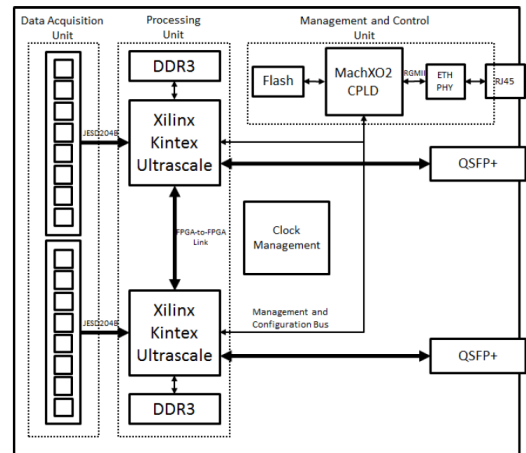


Figure 3. Block diagram showing the main functional parts of the ADU board.

3. Signal Processing Firmware for LFAA

Each board processes the signal from 16 antennas, two polarizations, combining them into a partial beam. 16 boards are connected together in a flexible way to form a 256 antennas station, using a general-purpose high-speed Ethernet interconnect. Signal processing for each antenna includes channelization, correction for cable mismatch, geometric delay¹, receiver amplitude and phase response, and atmospheric and polarization calibrations. Processing is shared among 2 FPGAs, each processing both polarizations for 8 antennas [3] (Fig. 4).

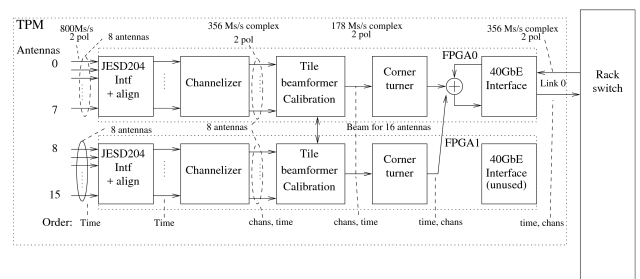


Figure 4. Signal processing chain inside one ADU board.

The ADCs sample the antenna signals at 8-bit, sampling rate of 800 MS/s nominal (range from 700 to 1000 MS/s). Samples are time tagged and synchronized, using an external clock and timing signal with sub-ps accuracy, and all commands to the board are applied at a specific sample. Beamforming is performed by channelizing the signals into 512 spectral channels, and applying a phase

¹ The geometric delay is due to the different time of arrival of the wave front on each individual antenna.

correction to each channel. Partial beams are stored in DDR memory, both to align them among boards and to assemble packets of contiguous time samples, one channel at a time. The complete beam is accumulated in a travelling packet that crosses the 16 iTPMs, and collects the sum of these partial beams. Beamformed samples are then organized into frames of one spectral channel, two polarizations and 2048 consecutive time samples, and sent to an interferometric correlator for further processing. The channelizer uses an oversampled polyphase filterbank architecture. Channels have a band of 926 kHz and are spaced 781 kHz. The filter bandpass is flat and free from aliasing in the central 781 kHz, thus allowing a seamless coverage of the input band. Minimum stopband rejection is 60 dB and increases to 87 dB over most of the band. The FFT uses a radix-4 architecture optimized for real signals.

Signal processing includes also:

- Static time domain delay correction
- Broadband total power calculation and interference detection
- Channelized data total power calculation
- Buffering raw antenna data in a 20 ms circular buffer

Firmware design is highly modular, with a board specific I/O ring containing the interfaces to the physical peripherals and the control structure, and a DSP core, with the signal processing chain. This eases the reuse of the processing blocks, assembled in a different DSP core, as for the PHAROS2 backend described below. The board is controlled using an AXI4lite bridge to the 1 GB Ethernet port, with each element seen as a memory mapped portion of the board address space. A map of this space is generated automatically at compile time, and used by the control software to address each element by name [4].

4. PHAROS2 digital backend

The ADU board is also proposed to be the digital acquisition and signal processing platform for PHAROS2 system [5]. PHAROS2 will be a C-band (4-8 GHz) cryogenically cooled low noise Phased Array Feed (PAF) demonstrator designed to be installed at the primary focus of the 76-m diameter Lovell radio telescope (Jodrell Bank Observatory, UK) for radio astronomy application. PHAROS2 is under development in the framework of the SKA PAF Advanced Instrumentation Program as an international collaboration.

The digital backend of PHAROS2 will implement a frequency domain beamformer capable of synthesizing four independent single-polarization beams on the sky by combining 24 active elements of an array of Vivaldi antennas. Each beam will cover an instantaneous IF bandwidth of ≈ 275 MHz across 375-650 MHz.

The functionality of such a digital system has many common parts with the one realized in the context of LFAA, so the idea is to reuse great part of the processing blocks already implemented.

The ADCs will work with a sampling rate of 700 MS/s, thus the 375-650 MHz band is sampled in the second Nyquist zone.

In this firmware design it is necessary to acquire 25 IF inputs: one is a calibration signal that has to be correlated against all the PAF antenna elements.

We are going to maintain the same oversampling polyphase filterbank architecture with 512 spectral channels (section 3): in this case channels have a bandwidth of 810 kHz and are spaced of 684 kHz.

Four beamforming blocks will be instantiated, each of them processing 24 single-polarization antenna elements and providing a beam (with ≈ 275 MHz bandwidth) with both integrated and non-integrated spectra. All the formed beams are then sent to the 40 GbE network and further processed by other computing nodes (CPU, GPU).

4.1 Preliminary Tests and Results

In September 2017, tests on the preliminary version of the firmware were performed with astronomical signals received by the BEST-2 array. BEST-2 is a subset of the Northern Cross radio telescope, located in Medicina (Bologna, Italy), and it consists of 8 East-West oriented cylindrical parabolic concentrators, each with 64 halfwave dipoles critically sampling a focal line at 408 MHz. These 64 dipoles are grouped in four 16-elements broadside sub-arrays, resulting in four receivers per cylinder, and a total of 32 effective receiving elements laid out on a 4-by-8 grid. A description of the overall system and the receivers is present in [6] and [7] respectively.

The ADU board was used only to sample and channelize a subset (24) of BEST-2 incoming IF signals (16 MHz of bandwidth centered at 30 MHz). Then, data were sent to a Workstation equipped with a solid state drive through high speed Ethernet interconnect. A pipelined off-line software running on the Workstation was used to realize a multi-beamformer on radio sources. This technique requires the accurate instrumental calibration of the receiver chains and the delay compensation that depends on the array geometry. The instrumental calibration (both in amplitude and phase) was carried out using the cross-correlations of the signals received from the bright compact radio source Cassiopeia-A (Cas-A). Up to five simultaneous beams equally spaced within the single element field of view (FoV) were produced. Initially only one spectral channel was stored and processed in order to validate the entire procedure. Then we extended the same method of calibration and beamforming to the maximum number of spectral channels (5) acquired and written correctly to the SSD without loss of packets. The E-Plane pointing direction and the Half Power Beam Width (HPBW) of the synthesized beams were measured by means of the transit of some strong calibration sources (Cassiopeia-A, Virgo-A, Taurus-A) over the array. These measurements are in quite good agreement with electromagnetic (EM) simulations both for the pointing ($\approx 0.1^\circ$ of error) and HPBW ($\approx 0.2^\circ$ of error). However, there is an asymmetry of the power pattern of the laterally steered beams. This effect seems more evident as beams

are more distant from the central one. We have not completely understood the cause of this difference and we are investigating the problem. Nevertheless, the tests have demonstrated the correct functioning of the firmware design in the ADU board.

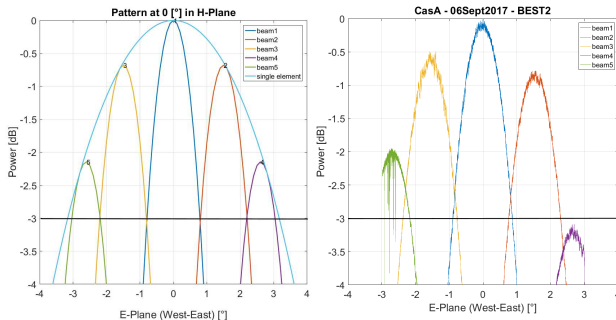


Figure 5. Beam patterns of five simultaneous beams generated within the single element FoV of BEST-2 array: comparison between the EM simulation (left) and measurement performed during the Cas-A transit occurred on 06 September 2017 (right).

5. Next Release of the Board and Future Developments

The purpose of increasing the number of iTPM boards in the LFAA cabinets and reducing power consumption is being pursued with the development of newer versions of both ADU and Pre-ADU boards. The two Pre-ADU boards of the current release of iTPM assembly will be implemented as a single board, receiving 32 analogue signals from the antennas. One Pre-ADU and one ADU board will be juxtaposed in the cabinet and connected by means of a suitable high-speed connector.

The main components of the ADU will be upgraded. The current FPGAs will be replaced by Xilinx 16 nm Kintex Ultrascale+ devices; the AD9680 ADCs will be substituted by AD9695 ADCs; DDR3L memories are going to be updated to the DDR4 family. The board will host sixteen memory chips, 8 Gbit each, with a 64-bit wide memory bus, for a total of 16 GByte memory.

Moreover, the bus between the two FPGAs will be implemented by using transceiver links, in place of previous normal LVDS lanes, allowing to double the data transfer rate.

Thanks to this evolution, the ADU board will maintain the original architecture, increase the performance/resources and reduce of about 20% the absorbed power.

In order to minimize cabling at cabinet level, a solution consisting of a backplane, implementing connections among iTPMs will be developed. This also allows for an easier installation/maintenance of the overall system.

6. Acknowledgements

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